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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,255	11/09/2001	Carl B. Frankel	5181-96400	2558
7590	08/16/2005			EXAMINER PROCTOR, JASON SCOTT
Lawrence J. Merkel Conley, Rose, & Tayon, P.C. P.O. Box 398 Austin, TX 78767			ART UNIT 2123	PAPER NUMBER

DATE MAILED: 08/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/008,255	FRANKEL ET AL.	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM  
 THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 16 May 2005.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 35-67 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 35-67 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 09 November 2001 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>5/16,7/25/02</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

## **DETAILED ACTION**

Claims 1-34 were presented for examination. Claims 1-34 were rejected in Office Action mailed on 18 March 2005. Applicants' response received on 16 May 2005 cancelled claims 1-34 and added new claims 35-67.

Claims 35-67 have been rejected.

### ***Response to Applicants' Remarks***

Applicants' response has cancelled all previously pending claims in the application, therefore all previous rejections are moot.

### ***Outstanding Objections and Rejections***

#### ***Claim Objections***

1. Claim 47 is objected to because of the following informalities: Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. Please see 37 CFR 1.75(i). Appropriate correction is required.

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 35-67 are rejected under 35 U.S.C. § 103(a) as being unpatentable over 5,881,267 to Dearth et al. (Dearth) supplied on Information Disclosure Statement filed on 25 February 2002 (reference A3) in view of "Structured Computer Organization, Second Edition" by Andrew S. Tanenbaum (Tanenbaum).

The Examiner notes that Dearth qualifies as prior art under 35 U.S.C. § 102(b) and is therefore not subject to the exclusions of 35 U.S.C. § 103(c).

Regarding claims 35, 47 and 60, Dearth discloses a distributed simulation system (FIG. 1; column 3, lines 61-64) comprising:

A plurality of nodes configured to simulate one of a plurality of electronic components of an electronic system under test [*"virtual bus stubs ("VBSs") 114A and 114B (FIG. 1) are included in simulation systems 116A and 116B, respectively, and collectively simulate a bus 214 (FIG. 2) which is connected between circuit parts 212A and 212B which in turn simulated by distributed simulation parts ("DSPs") 112A (FIG. 1) and 112B"*, (column 4, lines 41-47)],

Wherein the plurality of nodes are configured to communicate during a simulation using a predefined grammar that includes transmit signal message packets, wherein a transmit signal message packet comprises signal values corresponding to electronic signals in the electronic system under test, the electronic signals providing communication between the plurality of electronic components included in the electronic system under test [*"With each simulated cycle of a clock of bus 214, a hub 110A (FIG. 1) (i) collects data which represents components of the simulated state of bus 204 (FIG. 2) from VBSs 114A (FIG. 1) and 114B, (ii) resolves the current*

*simulated state of bus 214 (FIG. 2) and (iii) sends data representing the resolved state of the simulated bus to VBSs 114A (FIG. 1) and 114B.” (column 4, lines 48-67); “the bus protocol is an inherent part of the design of each of DSPs 112A (FIG. 1) and 112B.” (column 5, lines 9-35)],*

Wherein a first node of the plurality of nodes is assigned a first electronic component of the plurality of electronic components for the distributed simulation [*“circuit parts 212A and 212B which in turn simulated by distributed simulation parts (“DSPs”) 112A (FIG. 1) and 112B.”* (column 4, lines 31-47)],

And wherein the first node further comprises code to interface to the hardware circuitry to provide input signal values received from other nodes of the plurality of nodes to the hardware circuitry and to capture output signal values driven by the hardware circuitry to provide the output signal values to the other nodes of the plurality of nodes [*“each circuit part has access to the simulated state of the bus through a respective virtual bus stub”* (column 3, lines 31-35); *“Thus, the state of the bus includes all the information regarding the state of the other circuit part beyond the state of the bus.”* (column 3, lines 36-59); *“In simulating circuits, simulation system 116A receives test data defining simulated signals to be applied to components of the circuit simulated by the model and produces result data which represents signals produced by the simulated circuit in response to the test data.”* (column 6, lines 33-52)], and

Wherein a second node of the plurality of nodes simulates a second electronic component of the plurality of electronic components [*“Simulation system 116B (FIG. 1) is directly analogous to simulation system 116A and the foregoing description of simulation system 116A is*

*equally applicable to simulation system 116B. Simulation system 116B includes DSP 112B which represents in HDL circuit part 212B (FIG. 2). ” (column 6, lines 53-67)].*

Dearth does not disclose a first node that comprises the first electronic component *implemented in hardware circuitry*, and a second node simulates the second component using a first simulation mechanism that *does not include hardware circuitry that implements the second electronic component*. Dearth’s disclosure states that the nodes of the distributed simulation system are essentially analogous but distinct computers (column 6, lines 53-67).

Tanenbaum teaches that “*Hardware and software are logically equivalent.*” (page 11).

Tanenbaum explains:

Any operation performed by software can also be built directly into the hardware and any instruction executed by the hardware can also be simulated in software. The decision to put certain functions in hardware and others in software is based on such factors as cost, speed, reliability, and frequency of expected changes. There are no hard and fast rules to the effect that X must go into the hardware and Y must be programmed explicitly. Designers with different goals may, and often do, make different decisions. (page 11)

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants’ invention to implement one or more of the distributed simulation nodes in hardware, as opposed to programmed software, for any number of reasons set forth by Tanenbaum. Additionally, if certain components of the circuit being simulated are already exist as implemented in hardware, the accuracy and reliability of the simulation could only be enhanced by incorporating those hardware components into the distributed simulation system. The combination could be achieved as described by Tanenbaum – replacing one of the distributed

simulation parts (“DSPs”) of Dearth with a hardware implementation that provides the same functionality.

Regarding claims 36, 48, and 61, Dearth discloses that the first simulation mechanism (of the second node) comprises a first simulator and a first model of the second electronic component [FIG. 1, references 116B and 112B; “*virtual bus stubs (“VBSs”) 114A and 114B (FIG. 1) are included in simulation systems 116A and 116B, respectively, and collectively simulate a bus 214 (FIG. 2) which is connected between circuit parts 212A and 212B which in turn simulated by distributed simulation parts (“DSPs”) 112A (FIG. 1) and 112B*”, (column 4, lines 41-47); “*Simulation system 116B includes DSP 112B which represents in HDL circuit part 212B (FIG. 2).*” (column 6, lines 65-67)].

Regarding claim 49, Dearth discloses that the first model [“*DSP 112B*” of FIG. 1] comprises one or more files also stored on the computer readable medium [FIG. 1, reference 104B MEMORY which contains 112B DSP].

Regarding claims 37-40, 50-53, and 62-65, Dearth discloses that the first model is a register-transfer level model, a behavioral model, a hardware verification language model, and described in a hardware description language that supports constructs for verification and an interface to one or more programming languages [“*Simulator system 116A can be, for example, the Cadence Verilog hardware simulator available from Cadence Design System, Inc. of San Jose, Calif.*” (column 6, lines 49-52); “*The model within simulation system 116A which*

*represents a simulated circuit is generally in the form of a hardware description language (“HDL”))” (column 6, lines 53-59); “Simulation system 116B (FIG. 1) is directly analogous to simulation system 116A and the foregoing description of simulation system 116A is equally applicable to simulation system 116B.” (column 6, lines 59-65)].*

Regarding claims 41-45, 54-58, and 66, Dearth discloses that the first simulation mechanism comprises one or more program which, when executed, model the second electronic component [*“virtual bus stubs (“VBSs”) 114A and 114B (FIG. 1) are included in simulation systems 116A and 116B, respectively, and collectively simulate a bus 214 (FIG. 2) which is connected between circuit parts 212A and 212B which in turn simulated by distributed simulation parts (“DSPs”) 112A (FIG. 1) and 112B”,* (column 4, lines 41-47); FIG. 1, reference 104B MEMORY contains 112B DSP (which models the second electronic component) and is executed by 102B PROCESSOR].

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to implement the compiled and executed software programs disclosed by Dearth in a variety of suitable programming languages. The decision to choose one programming language over another does not constitute invention. Equivalent programs written in different programming languages produce functionally equivalent sets of machine instructions. The decision to choose one language over another is often based upon the programmer's personal skill set. Therefore it would have been obvious to program the system disclosed by Dearth in C, C++, or a portable, object-oriented programming language as motivated by the programmer's knowledge of those particular languages.

Regarding claims 46, 59, and 67, Dearth does not disclose that the first simulation mechanism includes an emulator configured to emulate the second electronic component using one or more programmable logic devices to model the hardware circuitry of the second electronic component.

However, such a limitation amounts to replacing software functionality with hardware functionality. Once programmed for a specific functionality, a programmable logic device acts as though it were hardware designed for that specific functionality. As set forth in the rejection of claims 35, 47, and 60, Tanenbaum teaches that "*Hardware and software are logically equivalent.*" (page 11).

It would have been obvious to a person of ordinary skill in the art to implement the first simulation mechanism using a programmable logic device because the logical equivalence of hardware and software is well known in the art. Motivation to do so is explicitly recited in Tanenbaum, such as the relative speed and reliability of a programmable logic device emulator as opposed to a software program. The combination could be achieved as described by Tanenbaum – replacing one of the distributed simulation parts (“DSPs”) of Dearth with a programmable logic device that is programmed to model the hardware circuitry of the second electronic component.

### ***Conclusion***

Art considered pertinent by the examiner but not applied has been cited on form PTO-892.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR)

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system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor  
Examiner  
Art Unit 2123

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A handwritten signature in black ink, appearing to read "J. P. Proctor".

LEO PICARD  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100